S03P1035 *Y00

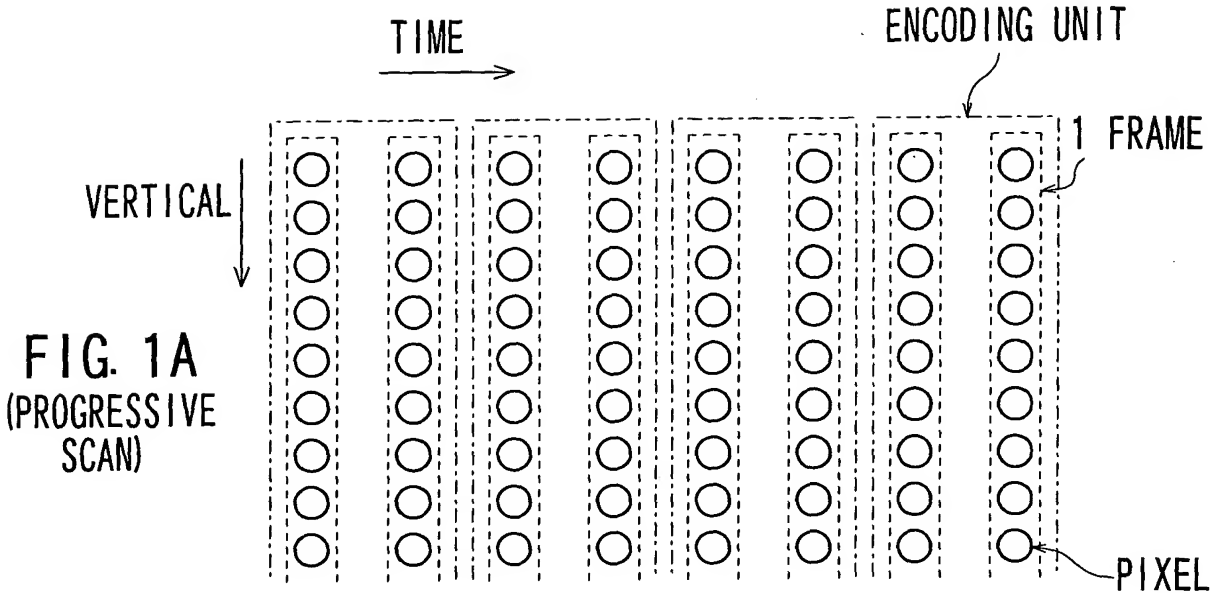


FIG. 1A
(PROGRESSIVE SCAN)

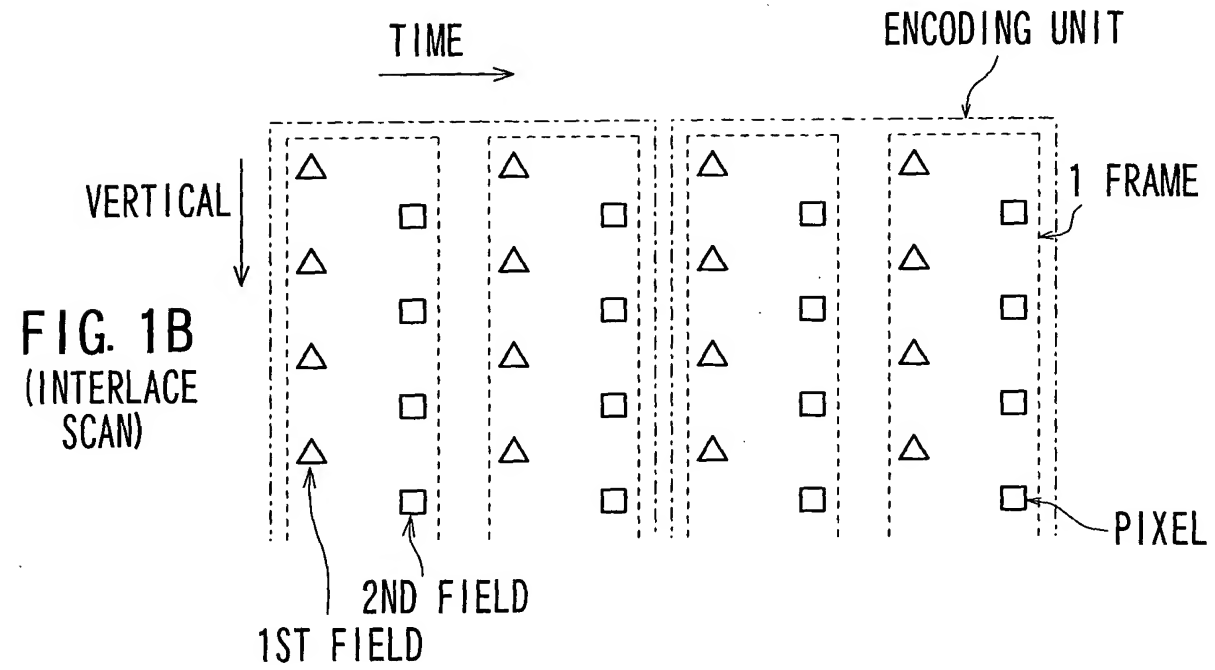


FIG. 1B
(INTERLACE SCAN)

FIG. 2

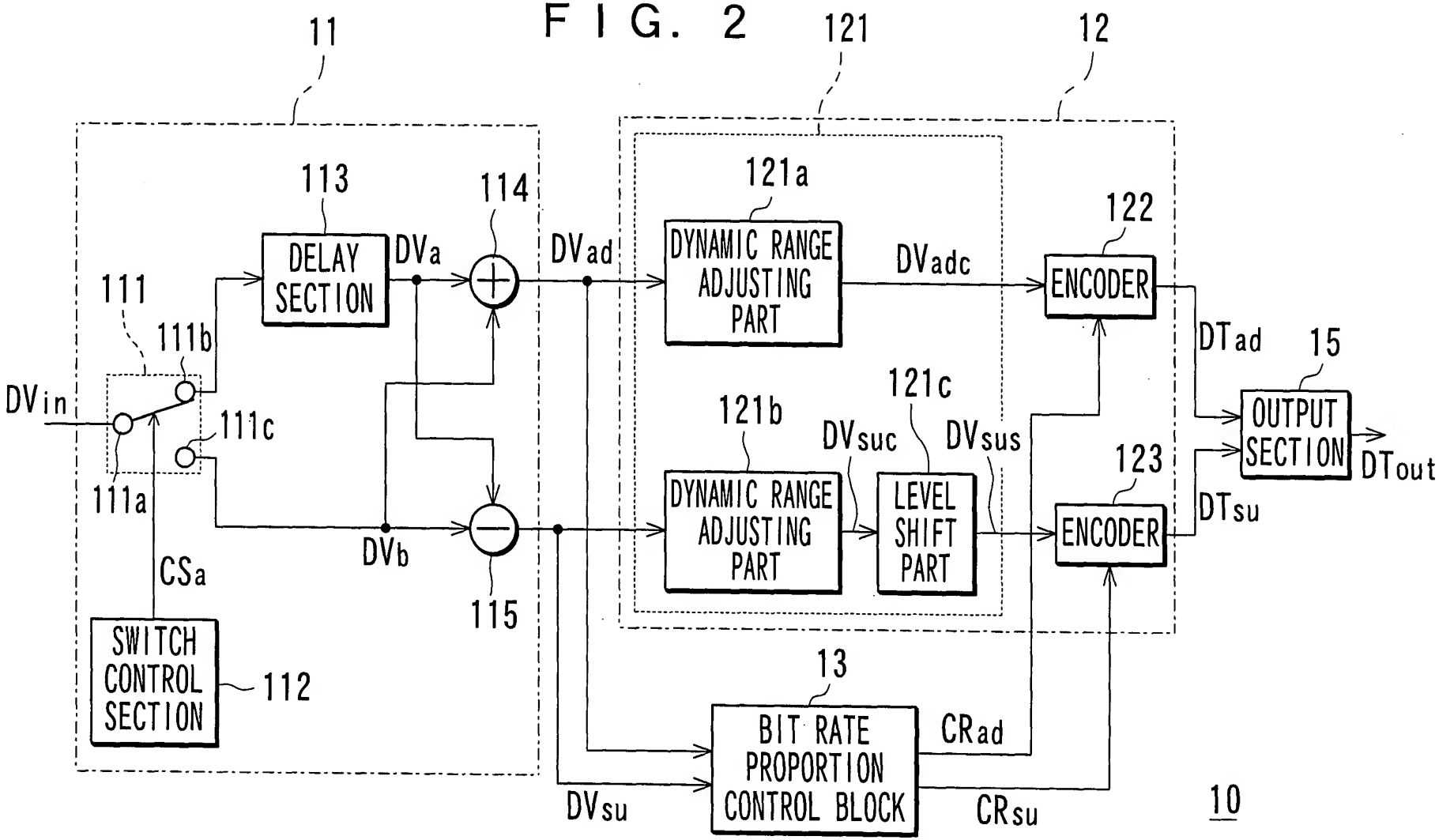

11
121
12
113
114
121a
122
DELAY SECTION
DVa
DVad
DYNAMIC RANGE ADJUSTING PART
DVadc
ENCODER
111
111b
DTad
15
DVin
121c
121b
DVsuc
DVsus
111c
OUTPUT SECTION
DTout
123
DYNAMIC RANGE ADJUSTING PART
LEVEL SHIFT PART
ENCODER
DTsu
111a
DVb
115
CSa
SWITCH CONTROL SECTION
112
13
BIT RATE PROPORTION CONTROL BLOCK
CRad
DVsu
CRsu
10

FIG. 3

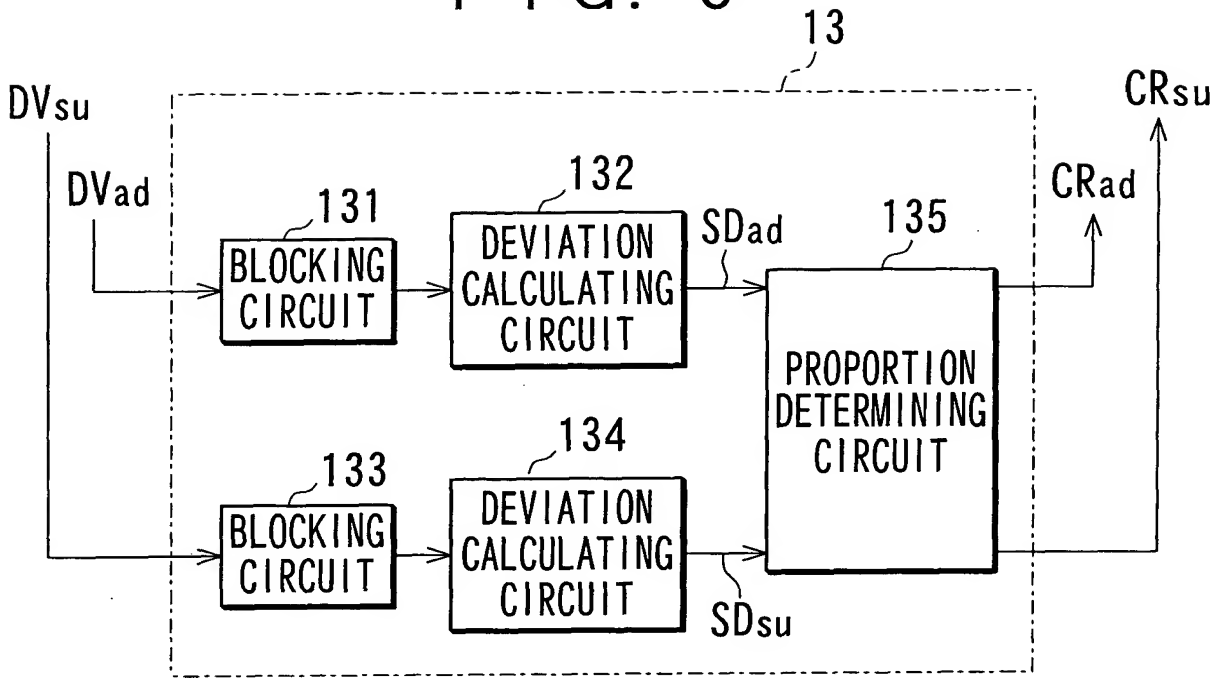

13
DVsu
DVad
131
BLOCKING CIRCUIT
132
DEVIATION CALCULATING CIRCUIT
SDad
135
PROPORTION DETERMINING CIRCUIT
CRad
CRsu
133
BLOCKING CIRCUIT
134
DEVIATION CALCULATING CIRCUIT
SDsu

FIG. 4

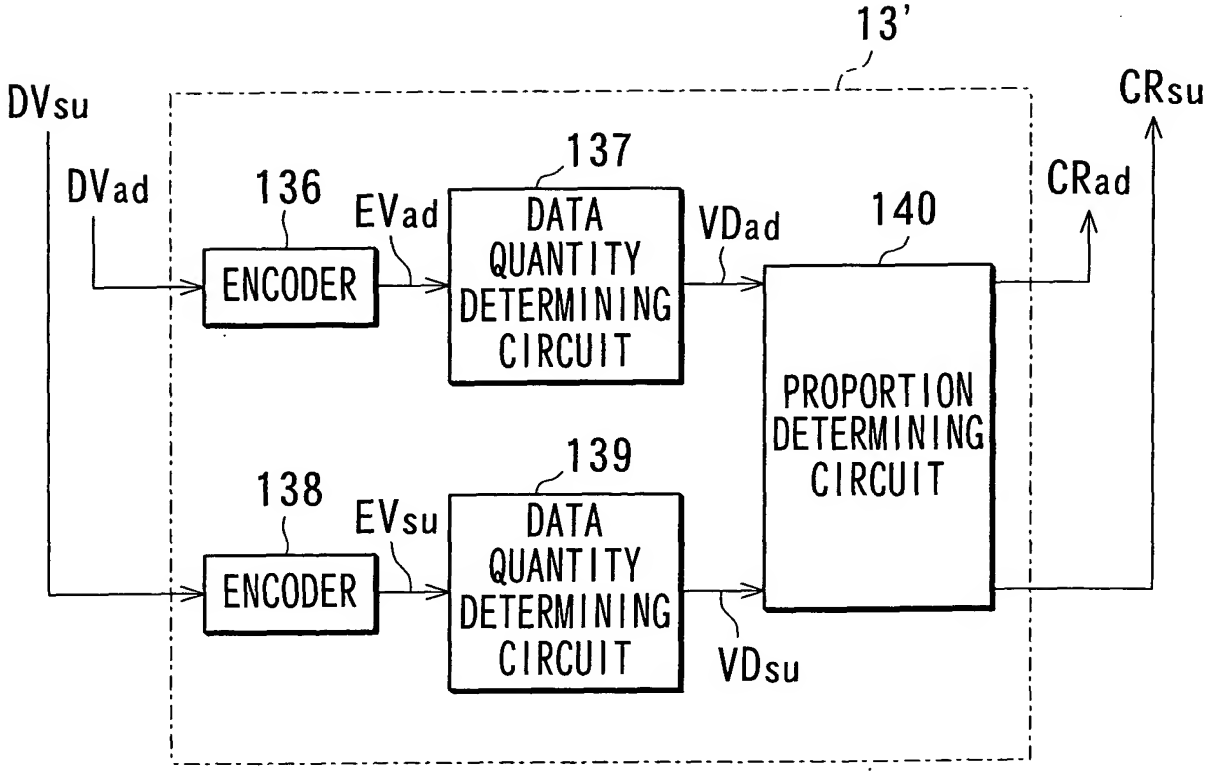

13'
DVsu
DVad
136
ENCODER
EVad
137
DATA QUANTITY DETERMINING CIRCUIT
VDad
140
PROPORTION DETERMINING CIRCUIT
CRad
CRsu
138
ENCODER
EVsu
139
DATA QUANTITY DETERMINING CIRCUIT
VDsu

FIG. 5

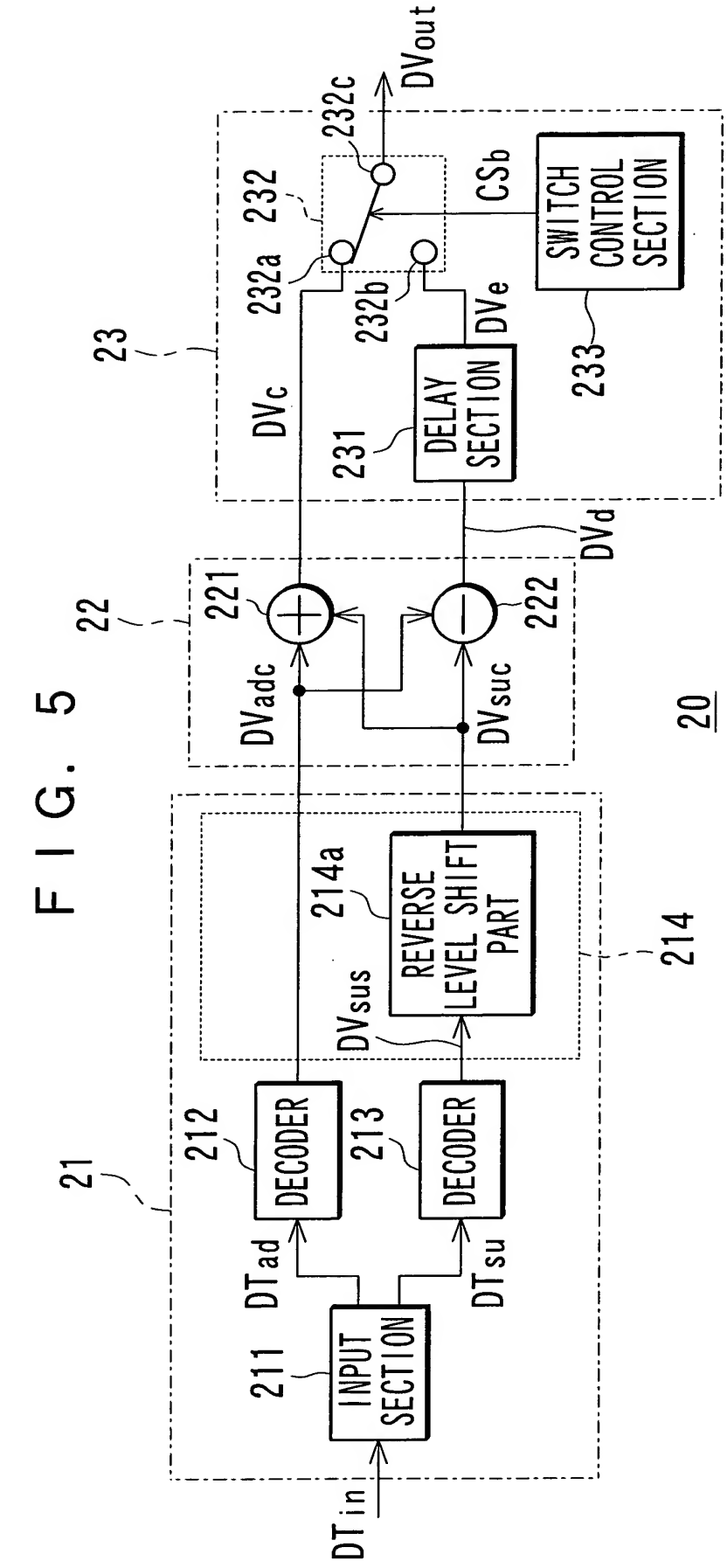

DTin
DTad
DTsu
211
INPUT SECTION
212
DECODER
213
DECODER
21
214
214a
REVERSE LEVEL SHIFT PART
DVsus
DVadc
DVsuc
22
221
222
DVd
23
DVc
231
DELAY SECTION
DVe
232
232a
232b
232c
CSb
233
SWITCH CONTROL SECTION
DVout
20

FIG. 6

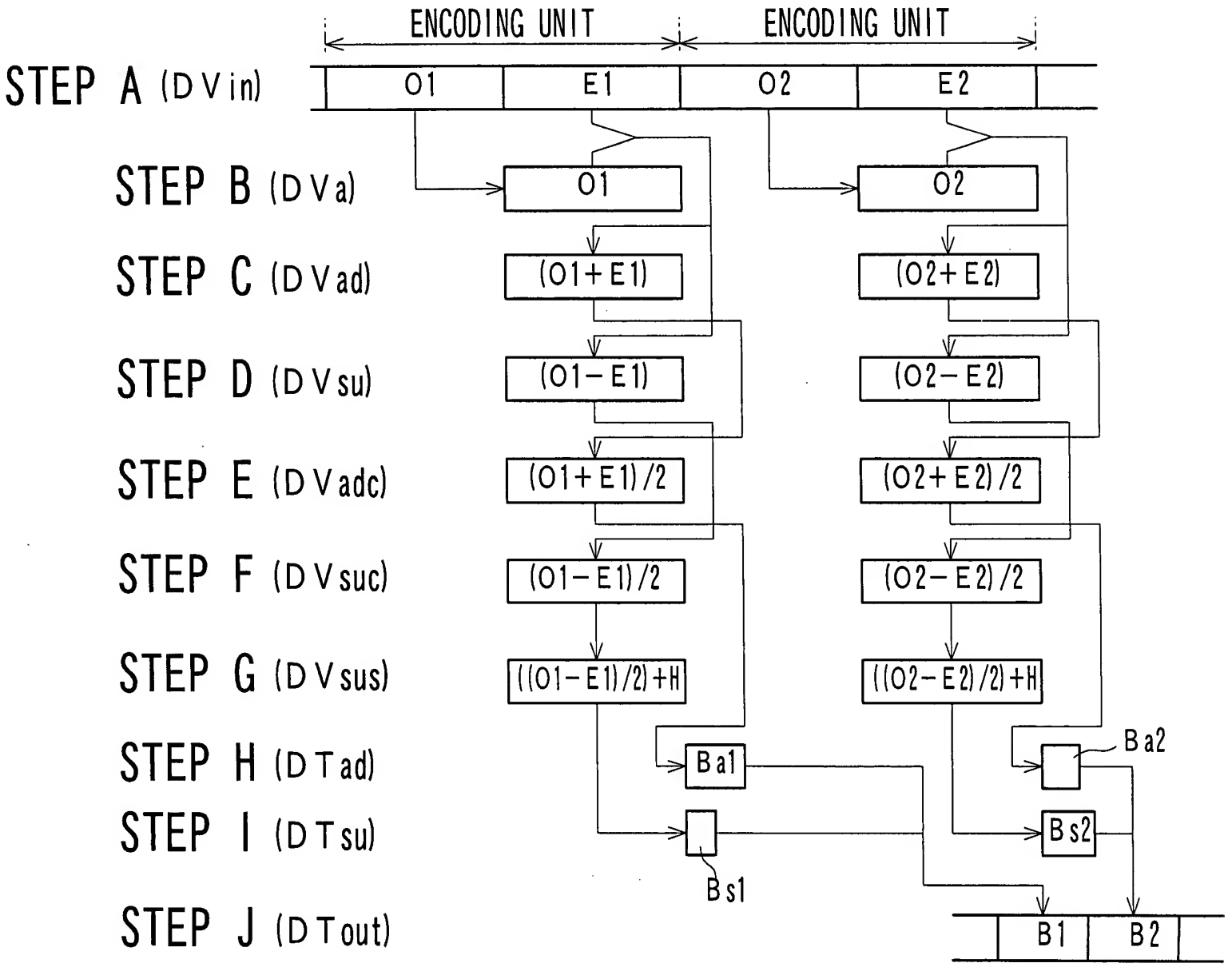

ENCODING UNIT
ENCODING UNIT
STEP A (DVin)
O1
E1
O2
E2
STEP B (DVa)
O1
O2
STEP C (DVad)
(O1+E1)
(O2+E2)
STEP D (DVsu)
(O1−E1)
(O2−E2)
STEP E (DVadc)
(O1+E1)/2
(O2+E2)/2
STEP F (DVsuc)
(O1−E1)/2
(O2−E2)/2
STEP G (DVsus)
((O1−E1)/2)+H
((O2−E2)/2)+H
STEP H (DTad)
Ba1
Ba2
STEP I (DTsu)
Bs1
Bs2
STEP J (DTout)
B1
B2

FIG. 7

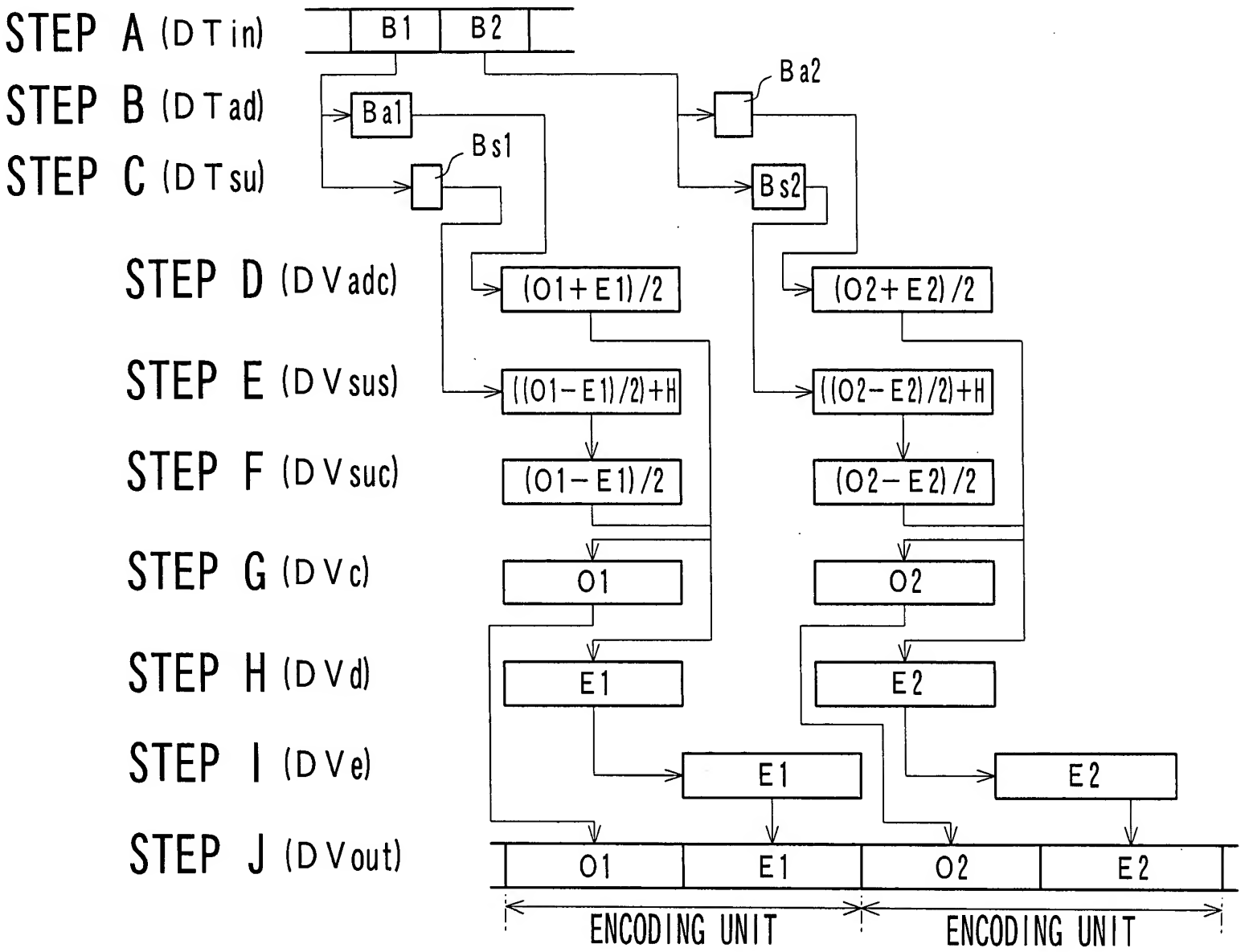

STEP A (DTin)
STEP B (DTad)
STEP C (DTsu)
STEP D (DVadc)
STEP E (DVsus)
STEP F (DVsuc)
STEP G (DVc)
STEP H (DVd)
STEP I (DVe)
STEP J (DVout)
B1
B2
Ba1
Ba2
Bs1
Bs2
(O1+E1)/2
(O2+E2)/2
((O1-E1)/2)+H
((O2-E2)/2)+H
(O1-E1)/2
(O2-E2)/2
O1
O2
E1
E2
E1
E2
O1
E1
O2
E2
ENCODING UNIT
ENCODING UNIT

FIG. 8

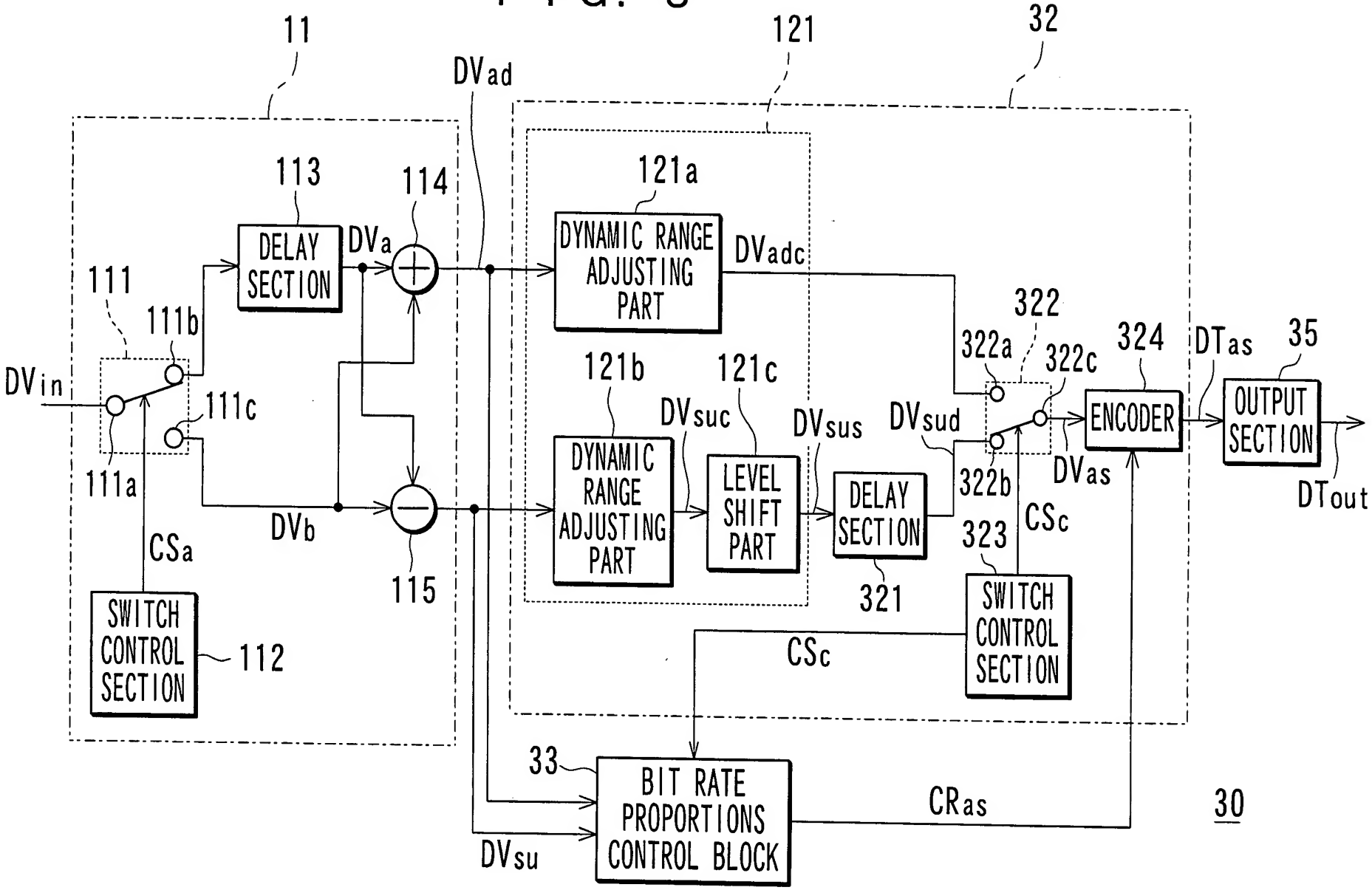

11
121
32
DVad
113
114
121a
DELAY SECTION
DVa
DYNAMIC RANGE ADJUSTING PART
DVadc
111
111b
322
322a
322c
324
DTas
35
DVin
121b
121c
111c
DVsuc
DVsus
DVsud
ENCODER
OUTPUT SECTION
111a
DYNAMIC RANGE ADJUSTING PART
LEVEL SHIFT PART
DELAY SECTION
322b
DVas
DTout
CSa
DVb
323
CSc
115
321
SWITCH CONTROL SECTION
112
CSc
SWITCH CONTROL SECTION
33
BIT RATE PROPORTIONS CONTROL BLOCK
CRas
30
DVsu

FIG. 9

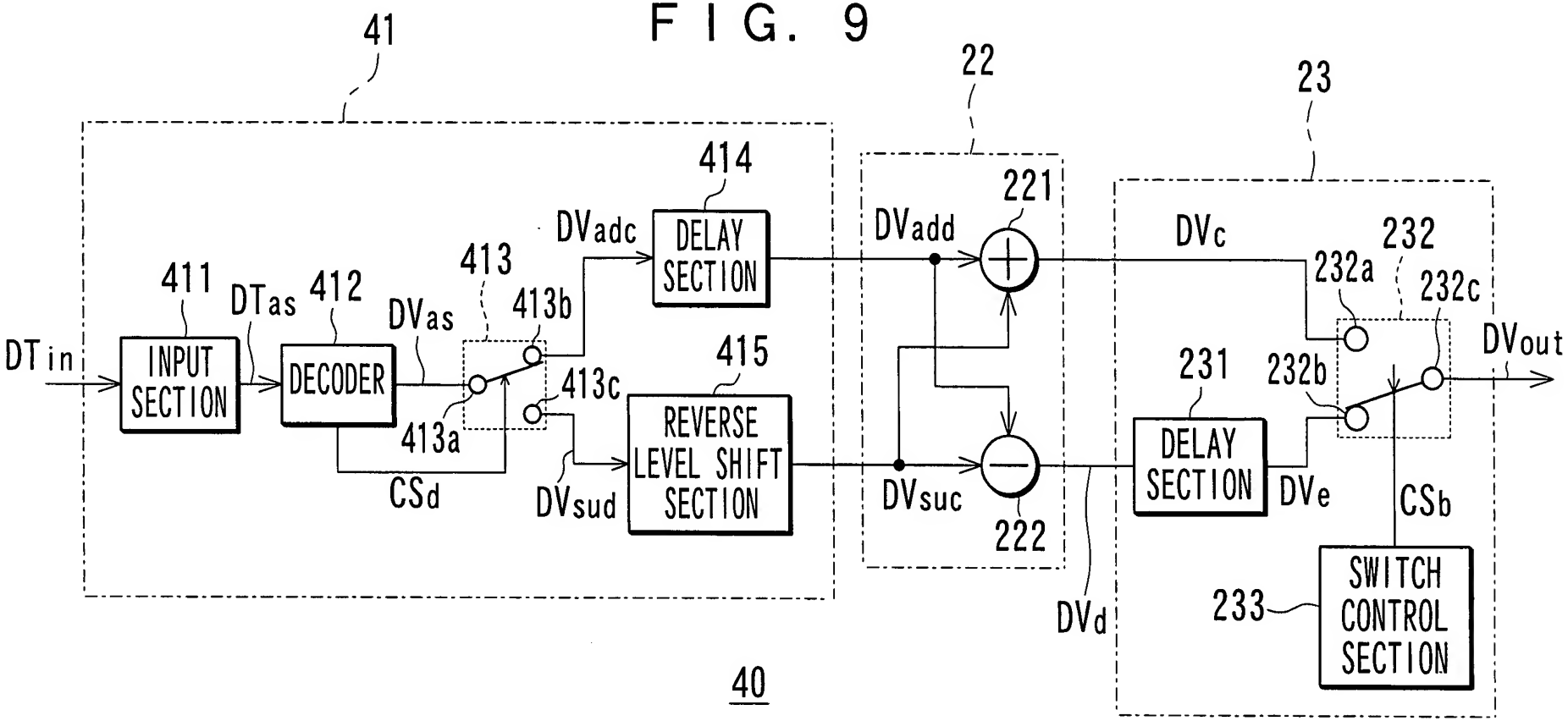

41
22
23
414
221
DVadc
DELAY SECTION
DVadd
DVc
232
232a
232c
411
DTas
412
413
413b
DVas
DTin
INPUT SECTION
DECODER
415
231
232b
DVout
413c
413a
REVERSE LEVEL SHIFT SECTION
DVsuc
DELAY SECTION
DVe
CSd
DVsud
222
CSb
SWITCH CONTROL SECTION
233
DVd
40

FIG. 10

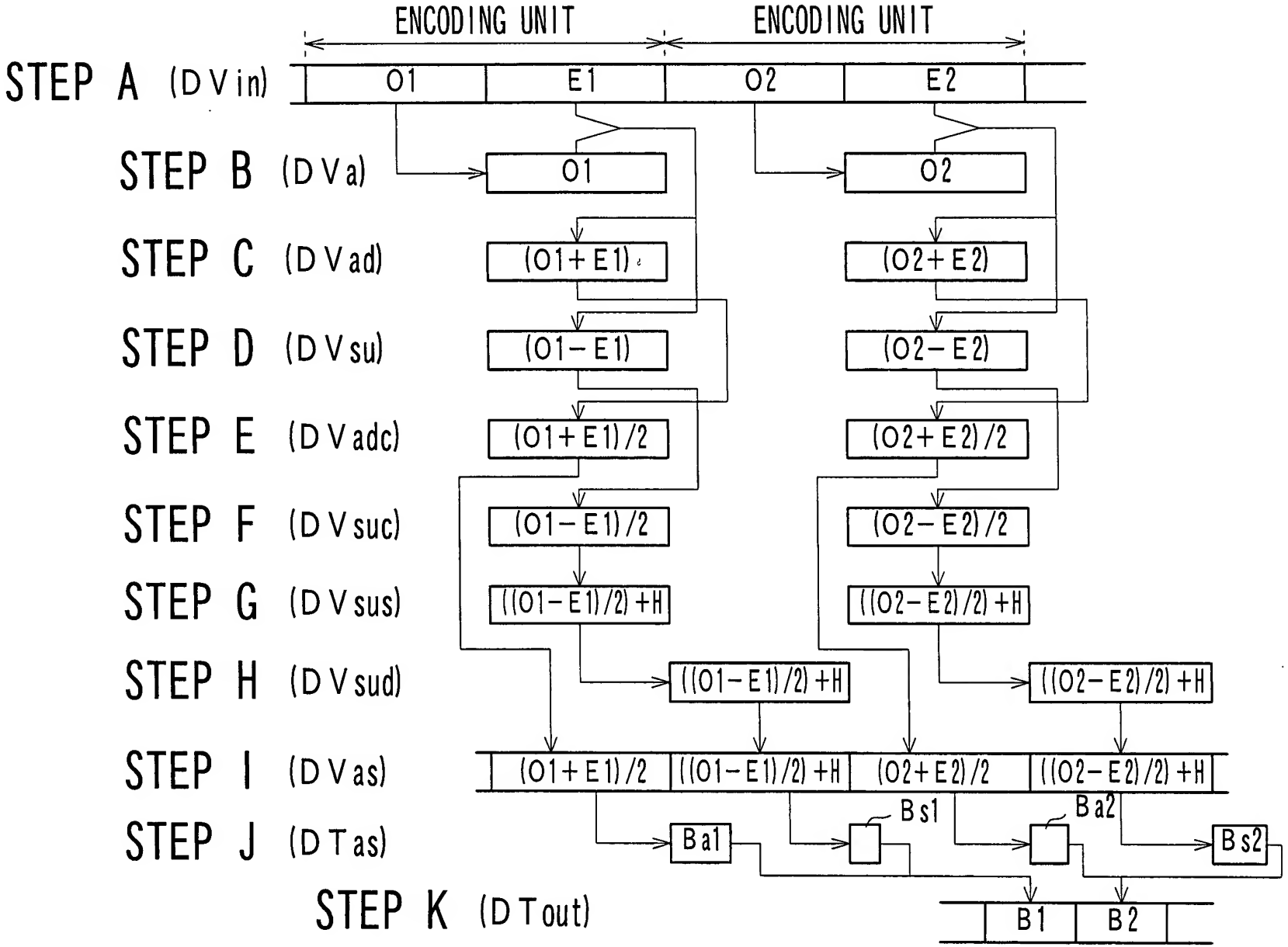

ENCODING UNIT
ENCODING UNIT
STEP A (DVin)
O1
E1
O2
E2
STEP B (DVa)
O1
O2
STEP C (DVad)
(O1+E1)
(O2+E2)
STEP D (DVsu)
(O1−E1)
(O2−E2)
STEP E (DVadc)
(O1+E1)/2
(O2+E2)/2
STEP F (DVsuc)
(O1−E1)/2
(O2−E2)/2
STEP G (DVsus)
((O1−E1)/2)+H
((O2−E2)/2)+H
STEP H (DVsud)
((O1−E1)/2)+H
((O2−E2)/2)+H
STEP I (DVas)
(O1+E1)/2
((O1−E1)/2)+H
(O2+E2)/2
((O2−E2)/2)+H
Bs1
Ba2
STEP J (DTas)
Ba1
Bs2
STEP K (DTout)
B1
B2

FIG. 11

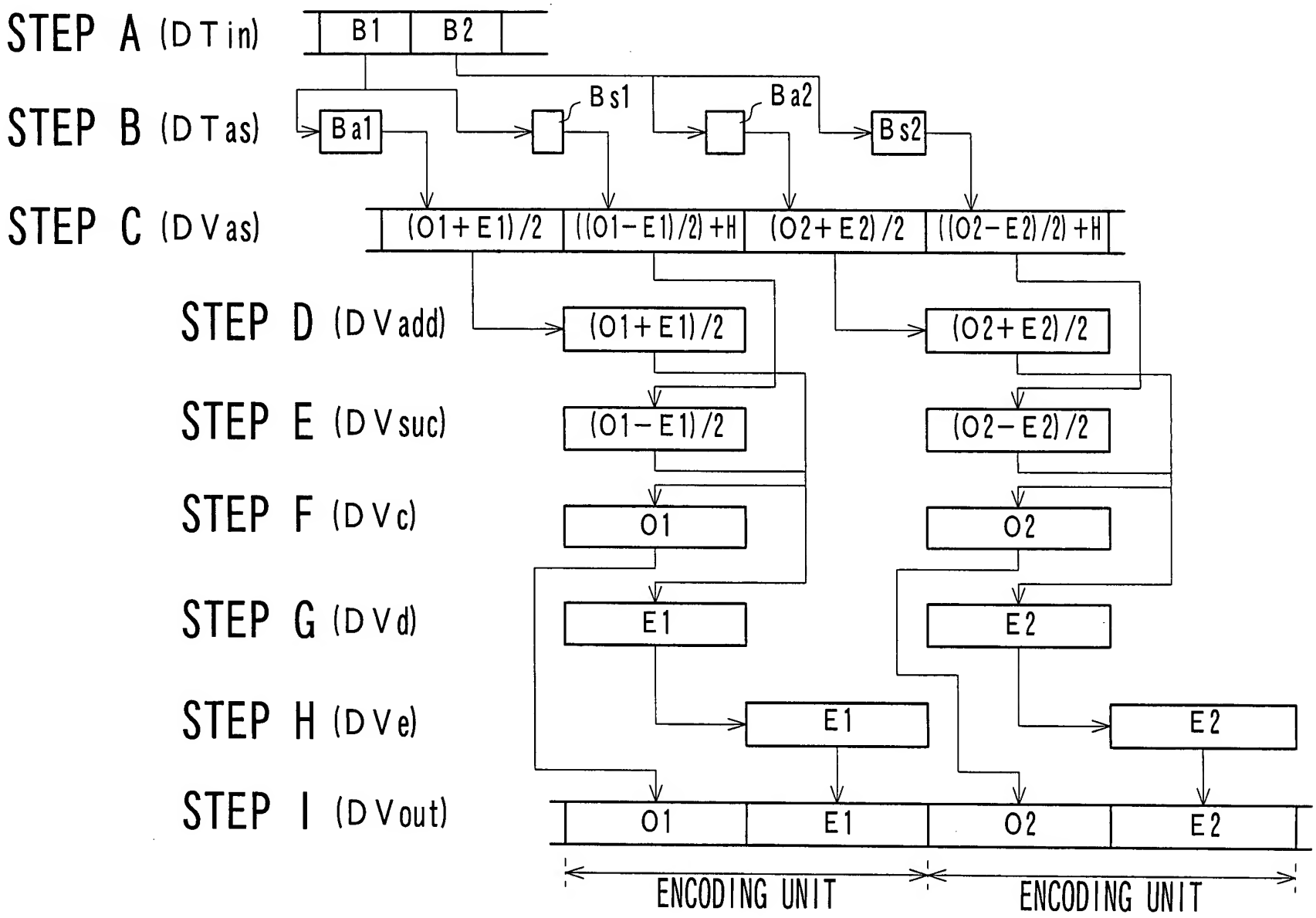

STEP A (DTin)
B1
B2
STEP B (DTas)
Ba1
Bs1
Ba2
Bs2
STEP C (DVas)
(O1+E1)/2
((O1−E1)/2)+H
(O2+E2)/2
((O2−E2)/2)+H
STEP D (DVadd)
(O1+E1)/2
(O2+E2)/2
STEP E (DVsuc)
(O1−E1)/2
(O2−E2)/2
STEP F (DVc)
O1
O2
STEP G (DVd)
E1
E2
STEP H (DVe)
E1
E2
STEP I (DVout)
O1
E1
O2
E2
ENCODING UNIT
ENCODING UNIT

FIG. 12

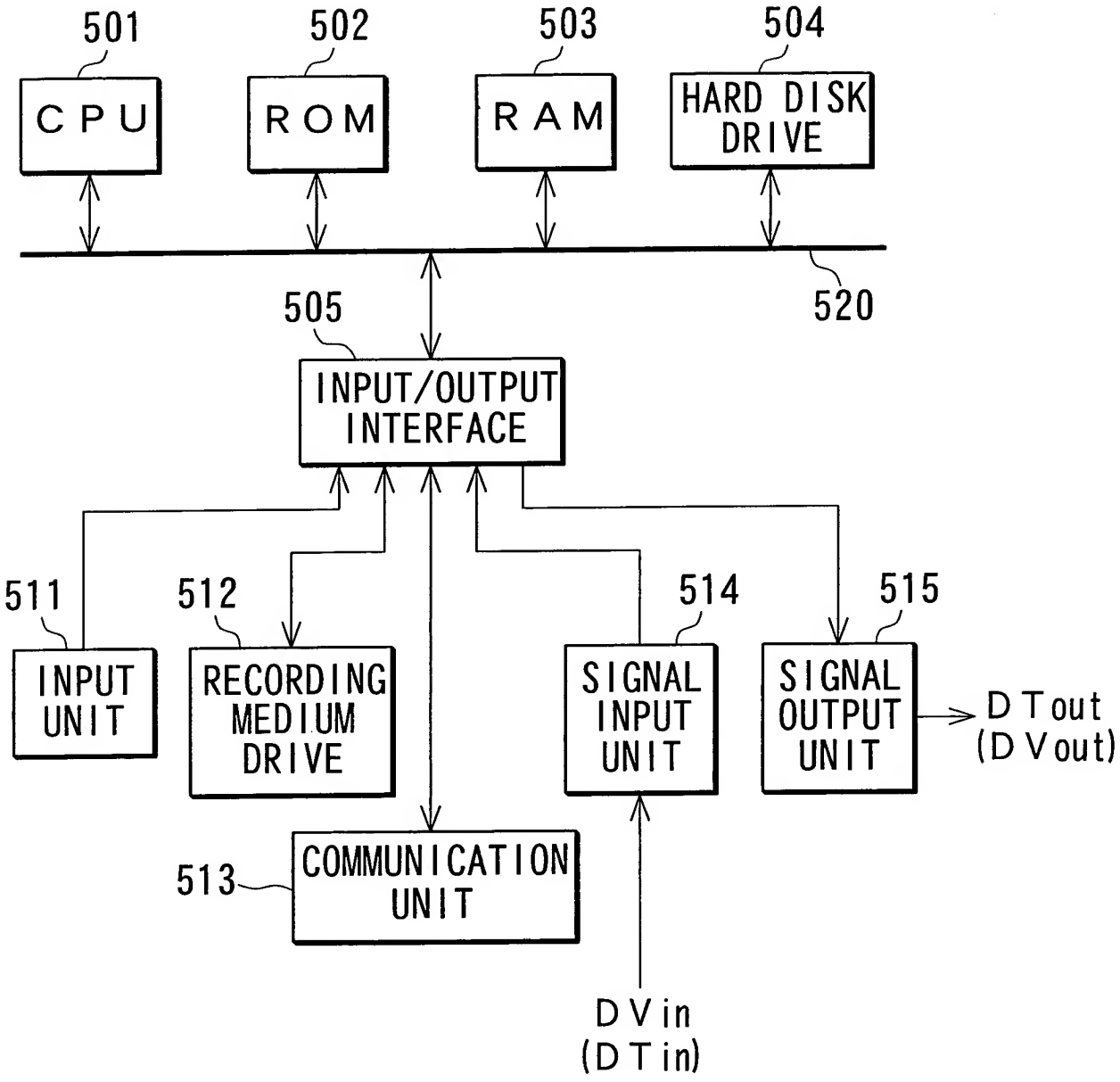

501
CPU
502
ROM
503
RAM
504
HARD DISK DRIVE
520
505
INPUT/OUTPUT INTERFACE
511
INPUT UNIT
512
RECORDING MEDIUM DRIVE
513
COMMUNICATION UNIT
514
SIGNAL INPUT UNIT
515
SIGNAL OUTPUT UNIT
DTout (DVout)
DVin (DTin)

FIG. 13

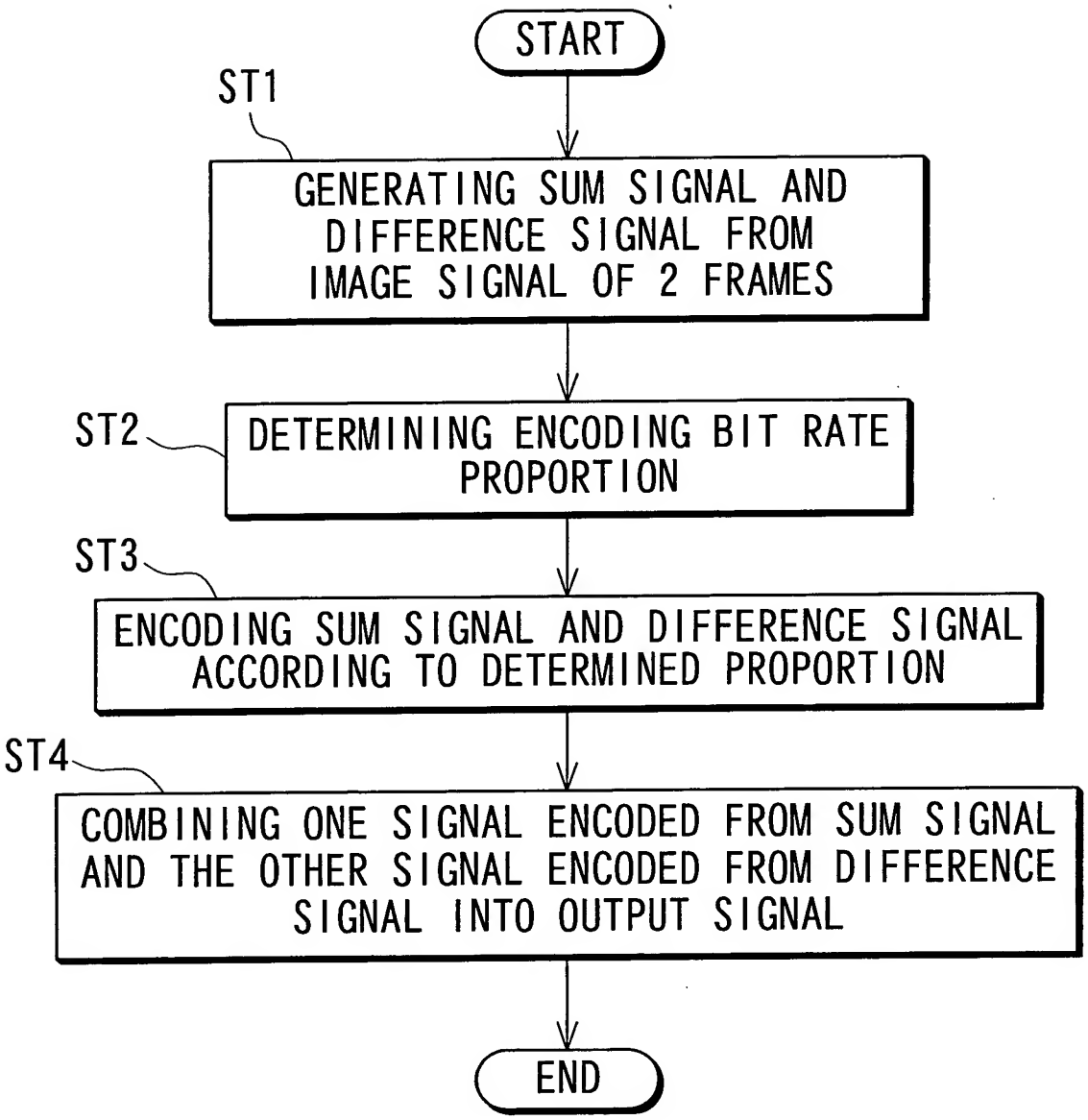
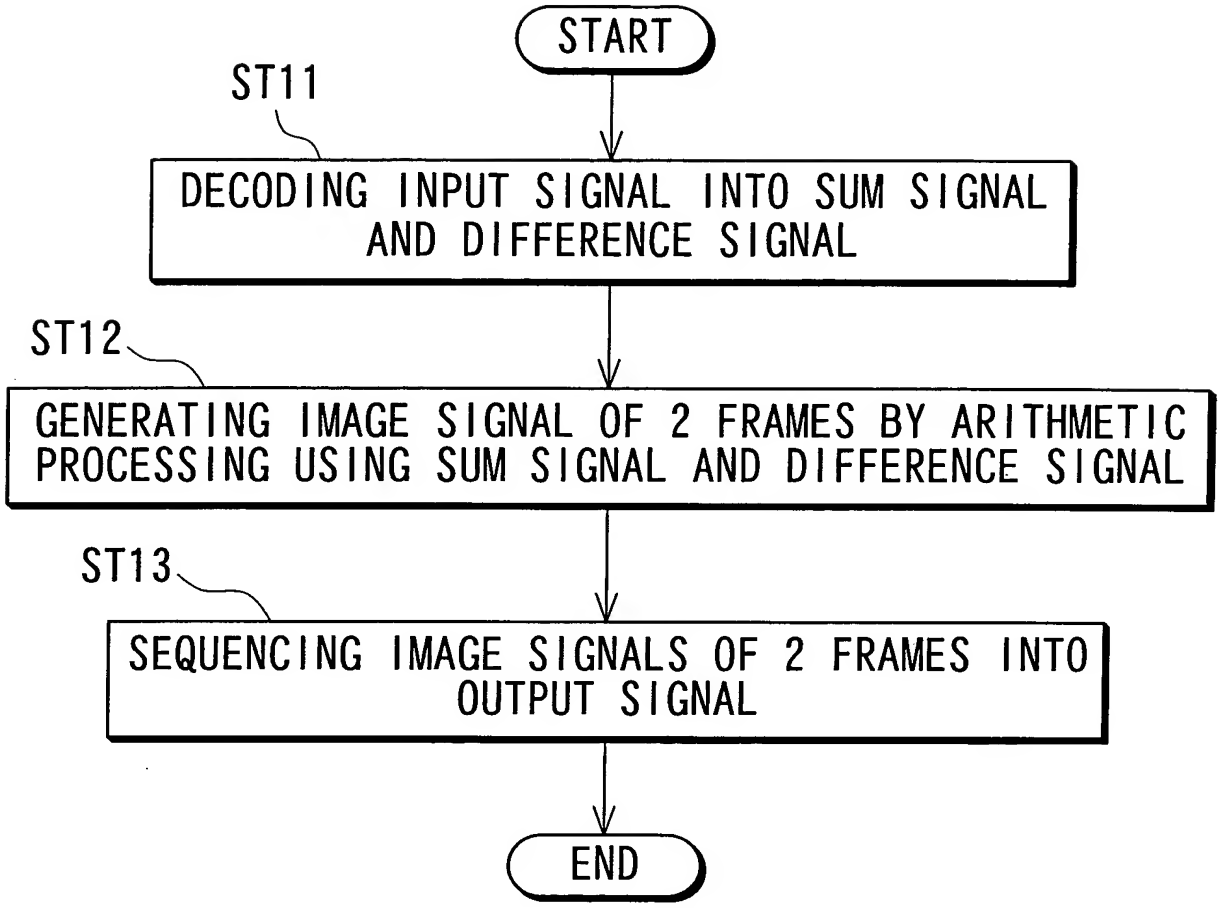

START
ST1
GENERATING SUM SIGNAL AND DIFFERENCE SIGNAL FROM IMAGE SIGNAL OF 2 FRAMES
ST2
DETERMINING ENCODING BIT RATE PROPORTION
ST3
ENCODING SUM SIGNAL AND DIFFERENCE SIGNAL ACCORDING TO DETERMINED PROPORTION
ST4
COMBINING ONE SIGNAL ENCODED FROM SUM SIGNAL AND THE OTHER SIGNAL ENCODED FROM DIFFERENCE SIGNAL INTO OUTPUT SIGNAL
END

FIG. 14


START
ST11
DECODING INPUT SIGNAL INTO SUM SIGNAL AND DIFFERENCE SIGNAL
ST12
GENERATING IMAGE SIGNAL OF 2 FRAMES BY ARITHMETIC PROCESSING USING SUM SIGNAL AND DIFFERENCE SIGNAL
ST13
SEQUENCING IMAGE SIGNALS OF 2 FRAMES INTO OUTPUT SIGNAL
END